100G QSFP28 ER4 Optical Transceiver

Part Number - VQ-1CER4CS-AA

VQ-1CER4CS-AA is a high performance QSFP28 transceiver module for 100 Gigabit Ethernet data links over single mode fiber.

Features

- QSFP28 Multi-Source Agreement compliant
- Hot pluggable QSFP28 footprint
- Supports 103.125 Gbps Data Rate
- 4 x 25.781Gbps Serial Electrical Interface (CEI-28G-VSR)
- Dual LC Connector
- 4 x cooled 1310nm LAN-WDM EML Transmitters
- 4 x PIN+SOA Receivers
- Up to 40km Point-to-Point Transmission on Single Mode Fiber
- Operating temperature range 0°C to 70°C
- Power Dissipation <5W
- Single +3.3V Power Supply

Applications

- 100GBASE-ER4 100G Ethernet

Ordering Information

Part Number	Description
VQ-1CER4CS-AA	QSFP28 ZR4, 1310nm LAN-WDM, Tx (EML), Rx (PIN+SOA), maximum distance 40km on SMF, 100 Gigabit Ethernet, dual LC connector, pull-tab, 5W, 0°C to 70°C, DDM

Product Overview

This transceiver is a high performance QSFP28 transceiver module for 100 Gigabit Ethernet data links over a single mode fiber pair. The maximum reach is 40km.

This module is compliant with the QSFP28 Multisource Agreement (MSA) and hot pluggable.

General Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Data Rate	DR		25.78		Gb/s	
Operating Temperature	TC	0		70	°C	1
Storage Temperature	TSTO	–40		85	°C	2
Input Voltage	VCC	3.14	3.3	3.46	V	3
Maximum Power Dissipation	PD			5.0	W	
Operating Distance				40	KM	

1.Case temperature
2.Ambient temperature
3.For electrical power interface

Optical – Transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Optical Center Wavelength (L0 Lane)	λC	1294.53	1295.56	1296.59	nm	
Optical Center Wavelength (L1 Lane)	λC	1299.02	1300.06	1301.09	nm	
Optical Center Wavelength (L2 Lane)	λC	1303.54	1304.59	1305.63	nm	
Optical Center Wavelength (L3 Lane)	λC	1308.09	1309.14	1310.19	nm	
Total Average Optical Output Power	PT			8.9	dBm	1,2
Average Output Power (Each Lane)	PTX	–2.9		2.9	dBm	1,2
Optical Modulation Amplitude (Each Lane)	OMA	0.1		4.5	dB	
Difference in launched Power (avg or OMA) between any two lanes	PTXdiff			3	dB	
Extinction Ratio	ER	8			dB	
Transmitter and Dispersion Penalty (Each Lane)	TDP			2.5	dB	

Notes:

1.Output power coupled into a 9/125 µm single mode fiber
2.Average launch power (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance

Optical- Receiver

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Optical Center Wavelength (L2 Lane)	λC	1303.54	1304.59	1305.63	nm	
Optical Center Wavelength (L3 Lane)	λC	1308.09	1309.14	1310.19	nm	
Average Receive Power (Each Lane)	PRX	–20.9		–3.5	dBm	
Receiver sensitivity (OMA)	RX_SEN1			–20.9	dBm	1

1.Measured with PRBS2 ^{31}-1 test pattern @ 25.78125Gbps, BER<1e-12

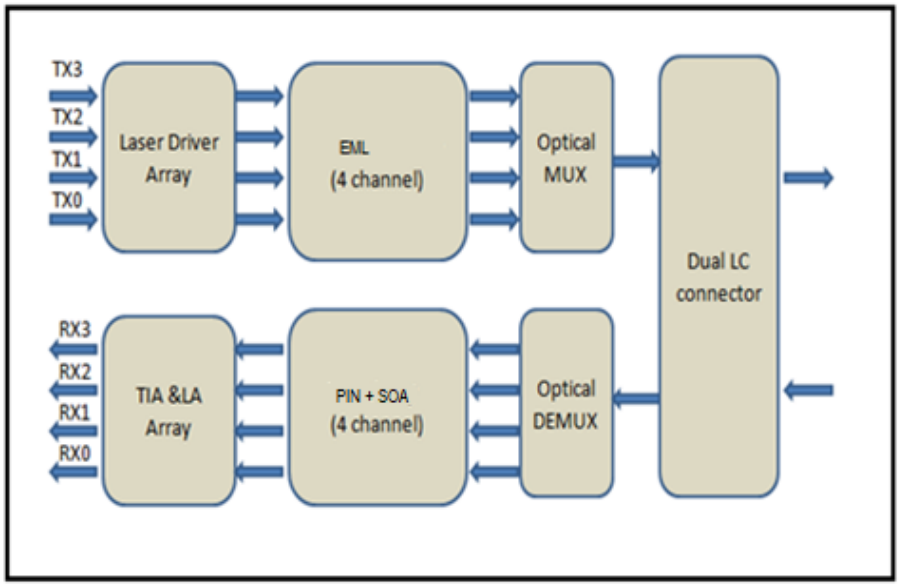
Electrical – Transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Input differential impedance	RIN		100		Ω	
Differential data input swing	VIN_PP	180		1000	mV	
Transmit disable voltage	VD	VCC–1.3		VCC	V	
Transmit enable voltage	VEN	VEE		VEE+0.8	V	

Electrical – Receiver

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Differential data output swing	VOUT_P	300		800	mV	
LOS Fault	VLOS_A	VCC–1.3		VCC	V	
LOS Normal	VLOS_D	VEE		VEE+0.8	V	

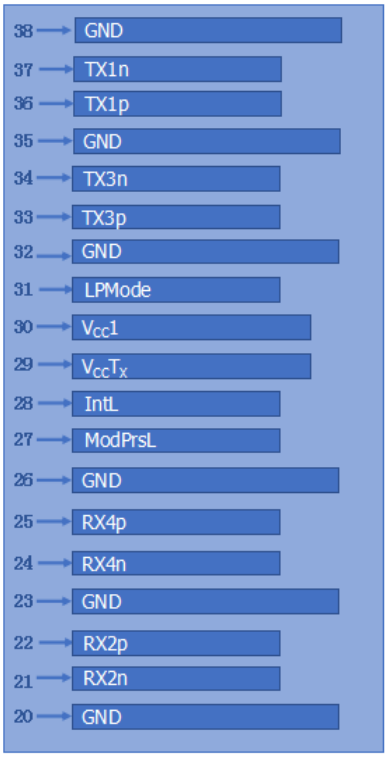
Transceiver Block Diagram



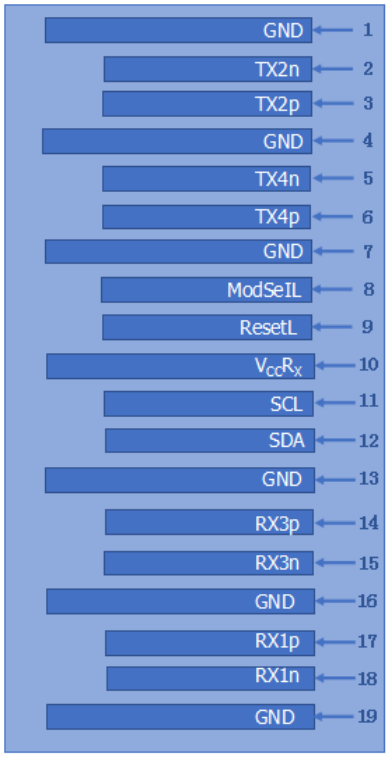
Functional Description

This product converts the 4-channel 25Gb/s electrical input data into LAN WDM optical signals. The light is combined by the MUX parts as a 100Gb/s data, propagating out of the transmitter module from the SMF. The receiver module accepts the 100Gb/s LAN WDM optical signals input, and de-multiplexes it into 4 individual 25Gb/s channels with different wavelength. Each wavelength light is collected by a discrete photo diode and amplified by a SOA, and then outputted as electric data after amplification by a TIA.

Electrical Connector Layout



Top Board



Bottom Board

Electrical Pin Definition

PIN #	Symbol	Description	Remarks
1	GND	Ground	5
2	Tx2n	Transmitter Inverted Data Input, LAN2	
3	Tx2p	Transmitter Non-Inverted Data Input, LAN2	
4	GND	Ground	5
5	Tx4n	Transmitter Inverted Data Input, LAN4	
6	Tx4p	Transmitter Non-Inverted Data Input, LAN4	
7	GND	Ground	5
8	ModSelL	Module select pin, the module responds to two-wire serial communication when low level	1
9	ResetL	Module Reset	2
10	$V_{CC}R_X$	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	5
14	Rx3p	Receiver Non-Inverted Data Output, LAN3	
15	Rx3n	Receiver Inverted Data Output, LAN3	
16	GND	Ground	5
17	Rx1p	Receiver Non-Inverted Data Output, LAN1	
18	Rx1n	Receiver Inverted Data Output, LAN1	
19	GND	Ground	5
20	GND	Ground	5
21	Rx2n	Receiver Inverted Data Output, LAN2	
22	Rx2p	Receiver Non-Inverted Data Output, LAN2	
23	GND	Ground	5
24	Rx4n	Receiver Inverted Data Output, LAN4	
25	Rx4p	Receiver Non-Inverted Data Output, LAN4	
26	GND	Ground	5
27	ModPrsL	The module is inserted into the indicate pin and grounded in the module	3
28	IntL	Interrupt	4
29	$V_{CC}T_X$	+3.3V Power Supply transmitter	
30	V_{CC1}	+3.3V Power Supply	
31	LPMode	Low Power Mode	5
32	GND	Ground	5

Notes:

1. ModSelL is the input pin. The module responds to 2-wire serial communication commands when it is held low by the host. ModSelL allows multiple QSFP modules to be used on a single 2-wire interface bus. If ModSelL is High, the module will not respond to any 2-wire interface communication from the host. ModSelL has internal pull-up resistors in the module
2. The module restart pin, when the low level on the ResetL pin lasts longer than the minimum pulse length, resets the module and restores all user modules to their default state. When performing reset device, the host should ignore all status bits. Until the module reset interrupt is completed, please note that during hot plugging, the module will issue this information to complete the reset interrupt without resetting
3. This pin is active high, indicating that the module is running under a low power module.
4. IntL is the output pin, which is the open collector output and must be pulled up to Vcc on the motherboard. When it is low, it indicates that the module may malfunction. The host uses a 2-wire serial interface to identify the interrupt source
5. Circuit ground is internally isolated from chassis ground.

References

1. IEEE standard 802.3bm. IEEE Standard Department
2. QSFP28 4X PLUGGABLE TRANSCEIVER – SFF-8665

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