100G QSFP28 LR4 Optical Transceiver

Part Number - VQ-1CLR4CS-AA

VQ-1CLR4CS-AA is a high performance QSFP28 transceiver module for 100 Gigabit Ethernet data links over single mode fiber.

Features

- 4x25G LAN-WDM optical architecture up to 103.1Gbps
- QSFP28 MSA compliant
- Up to 10km transmission
- Duplex LC connector
- Power dissipation < 3.5W
- Built-in digital diagnostic functions
- RoHS compliant
- Operating temperature range: 0◦C to 70◦C

Applications

- 100G Base LR4 100G Ethernet

Ordering Information

Part Number	Description
VQ-1C-LR4CS-AA	100G QSFP28 LC Connectors, Up to 10km on SMF, with DOM function

Product Overview

Vitex VQ-1C-LR4CS-AA optical transceivers are based on 100G Ethernet IEEE 802.3ba standard. The QSFP28 transceiver converts 4 inputs channels of 25Gb/s electrical data to 4 LAN-WDM optical signals and multiplexes them into a single channel for 100Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 100Gb/s input into 4 LAN-WDM channels signals and converts them to 4 channel output electricaldata.

General Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Bit Error Rate	BER			10^{-12}		
Operating Temperature	T_C	0		70	°C	1
Storage Temperature	T_{STO}	-40		85	°C	2
Input Voltage	V_{CC}	3.14	3.3	3.46	V	
Maximum Voltage	V_{MAX}	-0.5		3.6	V	3
Module total power	P			3.5	W	

1.Case temperature
2.Ambient temperature
3.For electrical power interface

Optical – Transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Signaling Speed per lane		25.78125±100ppm			Gb/s	
Total Output Optical Power	P_T			8.3	dBm	1
Average Launch Power (Each Lane)	P_{TX}	-4.3		4.5	dBm	
Optical Center Wavelength (L0 Lane)	λ_C	1294.53	1295.56	1296.59	nm	
Optical Center Wavelength (L1 Lane)	λ_C	1299.02	1300.06	1301.09	nm	
Optical Center Wavelength (L2 Lane)	λ_C	1303.54	1304.59	1305.63	nm	
Optical Center Wavelength (L3 Lane)	λ_C	1308.09	1309.14	1310.19	nm	
Optical Modulation Amplitude(Each Lane)	OMA	-1.3		4.5	dB	
Extinction Ratio	ER	4			dB	
Side Mode Suppression Ratio	SMSR	30			dB	
Relative Intensity Noise	RIN			-130	dB/Hz	
Transmitter Dispersion Penalty	TDP			1.8	dB	
Optical Return Loss Tolerance				20	dB	
Transmitter Eye Mask		Compliant with IEEE 802.3ba				

1.Average

Optical- Receiver

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Signaling Speed per lane		25.78125±100ppm			Gb/s	
Optical Center Wavelength (L0	λ_C	1294.5	1295.5	1296.5	nm	
Optical Center Wavelength (L1	λ_C	1299.0	1300.0	1301.0	nm	
Optical Center Wavelength (L2	λ_C	1303.5	1304.5	1305.6	nm	
Optical Center Wavelength (L3	λ_C	1308.0	1309.1	1310.1	nm	
Optical Input Power, each lane	P_{RX}	-10.6		-4.5	dBm	
Receiver Sensitivity (OMA), each Lane	R_{X_SEN} 1			-8.6	dBm	
LOS Assert	LOSA		-18		dBm	
LOS De-Assert	LOSD		-16		dBm	
LOS Hysteresis	LOSH	1.5			dB	

1. Average
2. Measured with PRBS2 ^{31}-1 test pattern @ 25.78125Gbps, BER<1e-12

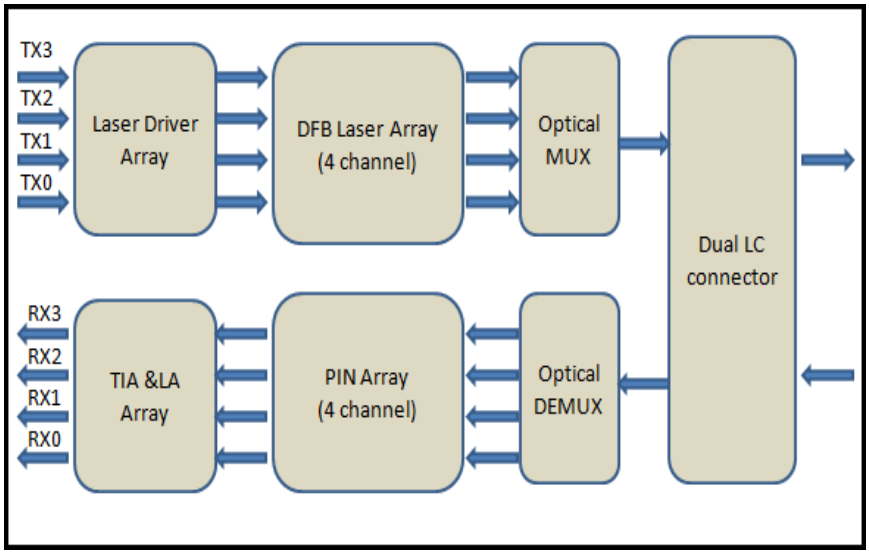
Electrical – Transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Signaling Rate per lane		25.78125±100ppm			Gb/s	
Differential data input swing	V_{IN_PP}			900	mV	
Transmit disable voltage	V_D	VCC-1.3		V_{CC}	V	
Transmit enable voltage	V_{EN}	V_{EE}		VEE+0.8	V	

Electrical – Receiver

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Signaling Rate per lane		25.78125±100ppm			Gb/s	
Differential data output swing	V_{OUT_P}	400		800	mV	
Data output rise time (20%-80%)	tr		12		ps	
Data output fall time (20%-80%)	tf		12		ps	
LOS Fault	LOSA	VCC-1.3		V_{CC}	V	
LOS Normal	LOSD	V_{EE}		VEE+0.5	V	

Transceiver Block Diagram

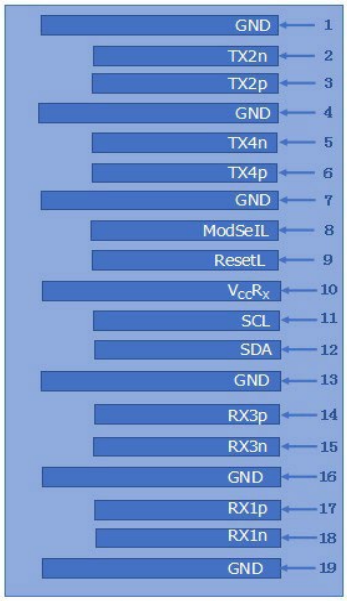


Functional Description

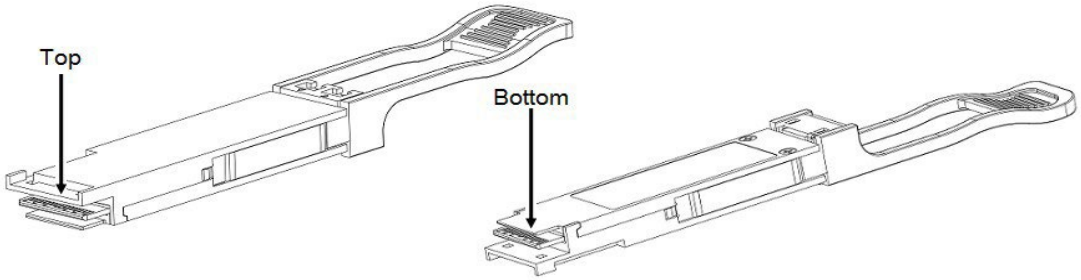
This product converts the 4-channel 25Gb/s electrical input data into LAN WDM optical signals (light), by a driven 4-wavelength Distributed Feedback Laser (DFB) array. The light is combined by the MUX parts as a 100Gb/s data, propagating out of the transmitter module from the SMF. The receiver module accepts the 100Gb/s LAN WDM optical signals input, and de-multiplexes it into 4 individual 25Gb/s channels with different wavelength. Each wavelength light is collected by a discrete photo diode, and then outputted as electric data after amplified by a TIA.

Electrical Connector Layout

Top of Board



Bottom of Board



Electrical Pin Definition

PIN #	Symbol	Description	Remarks
1	GND	Ground	5
2	Tx2n	Transmitter Inverted Data Input, LAN2	
3	Tx2p	Transmitter Non-Inverted Data Input, LAN2	
4	GND	Ground	5
5	Tx4n	Transmitter Inverted Data Input, LAN4	
6	Tx4p	Transmitter Non-Inverted Data Input, LAN4	
7	GND	Ground	5
8	ModSelL	Module select pin, the module responds to two-wire serial communication when low level	1
9	ResetL	Module Reset	2
10	$V_{CC}R_X$	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	5
14	Rx3p	Receiver Non-Inverted Data Output, LAN3	
15	Rx3n	Receiver Inverted Data Output, LAN3	
16	GND	Ground	5
17	Rx1p	Receiver Non-Inverted Data Output, LAN1	
18	Rx1n	Receiver Inverted Data Output, LAN1	
19	GND	Ground	5
20	GND	Ground	5
21	Rx2n	Receiver Inverted Data Output, LAN2	
22	Rx2p	Receiver Non-Inverted Data Output, LAN2	
23	GND	Ground	5
24	Rx4n	Receiver Inverted Data Output, LAN4	
25	Rx4p	Receiver Non-Inverted Data Output, LAN4	
26	GND	Ground	5
27	ModPrsL	The module is inserted into the indicate pin and grounded in the module.	3
28	IntL	Interrupt	4
29	$V_{CC}T_X$	+3.3V Power Supply transmitter	
30	$V_{CC}1$	+3.3V Power Supply	
31	LPMode	Low Power Mode	5
32	GND	Ground	5

Notes:

1. ModSelL is the input pin. The module responds to 2-wire serial communication commands when it is held low by the host. ModSelL allows multiple QSFP modules to be used on a single 2-wire interface bus. If ModSelL isHigh, the module will not respond to any 2-wire interface communication from the host. ModSelL has internal pull-up resistors in the module
2. The module restart pin, when the low level on the ResetL pin lasts longer than the minimum pulse length, resets the module and restores all user modules to their default state. When performing reset device, the host should ignore all status bits. Until the module reset interrupt is completed, please note that during hot plugging, the module will issue this information to complete the reset interrupt withoutresetting
3. This pin is active high, indicating that the module is running under a low power module.
4. IntL is the output pin, which is the open collector output and must be pulled up to Vcc on the motherboard. When it is low, it indicates that the module may malfunction. The host uses a 2-wire serial interface to identify the interrupt source
5. Circuit ground is internally isolated from chassisground.

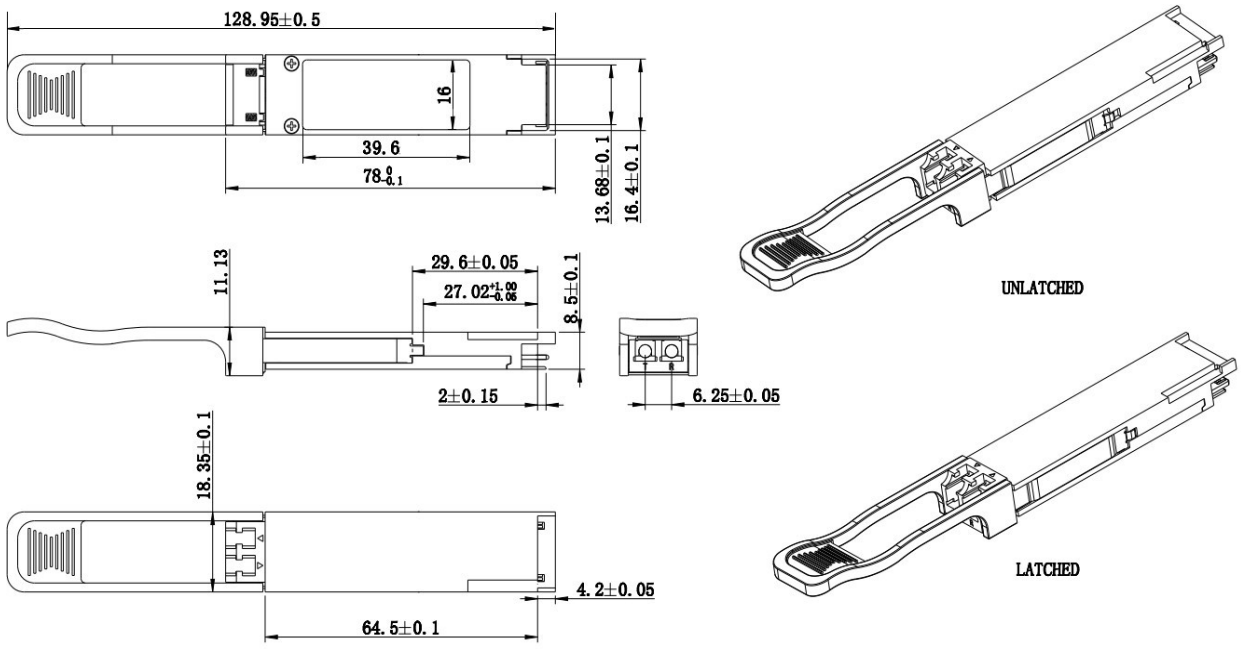
References

1. IEEE standard 802.3ba. IEEE Standard Department.
2. QSFP28 4X PLUGGABLE TRANSCEIVER –SFF-8665

Mechanical Dimensions

Module Weight: 38g

Dust Cap eight: .95g



ALL DIMENSIONS （NOT INCLUDING THE LENGTH OF THE CABLE）ARE ±0.2mm UNLESS OTHERWISE SPECIFIED

UNIT: mm

Contact Information

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