40G/100G QSFP28 SR4 Optical Transceiver

Part Number - VQ-1CSR4CP-GA

VQ-1CSR4CP-GA is a high performance QSFP28 transceiver module for use in dual rates 100Gb/s and 40Gb/s links over multimode fiber.

Features

- Compliant with IEEE Std 802.3bm,100G BASE SR4 Ethernet, 40G BASE SR4 Ethernet
- Compliant with QSFP28 MSA
- Management interface specifications per SFF-8636
- Single MPO connector receptacle
- 4 channels 850nm VCSEL array
- 4 channels PIN photo detector array
- Up to 103.1Gb/s data rates
- Quad 25G CDR, auto bypass at 40G application
- Single +3.3V power supply
- Class 1 laser safety certified
- Commercial operating temperature:0ºC to +70ºC
- Up to 70m on OM3 MMF and 100m on OM4 MMF
- RoHS6 Compliant

Applications

- 100G BASE-SR4 Ethernet
- 40G BASE-SR4 Ethernet
- Data Center

Ordering Information

Part Number	Data Rate	Link Length	Laser	Detector	Fiber Type	Temperature
VQ-1CSR4CP-GA	40G/100G	70m OM3 100m OM4	850nm VCSEL	PIN	SMF	0 – 70°C

Product Overview

Vitex **VQ-1CSR4CP-GA** transceivers are designed for use in dual rate 100Gb/s and 40Gb/s links over multimode fiber. They integrate four channel VCSEL array and four channel PIN photodiode array. The module can operate at 103.1Gb/s and 41.2Gb/s up to 70m using OM3 or 100m using OM4 MMF. They are compliant with the QSFP28 MSA and IEEE 802.3bm 100GBASE-SR4.

VQ-1CSR4CP-GA is compliant with RoHS.

General Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
Operating Temperature	Tc	0	25	70	°C	1
Storage Temperature	Ts	-40		85	°C	2
Input Voltage	Vcc	3.135	3.3	3.465	V	
Maximum Voltage	Vmax	-0.5		4.0	V	3
Module total power	Pt			2.5	W	
Module Low Power Mode	Plp			1.5	W	

1.Case temperature
2.Ambient temperature
3.For electrical power interface

Optical – Transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Note
Launch Optical Power	P	-8.4	-	+2.4	dBm	1
Center Wavelength Range	λc	840	850	860	nm	-
Extinction Ratio	EX	2	-	-	dB	2
Power Budget	-	8.2	-	-	dB	
Spectral width(RMS)	Δλ	-	-	0.6	nm	
Transmitter and Dispersion Penalty	TDP	-	-	4.3	dB	-
Optical Return Loss Tolerance	ORLT	-	-	12	dB	-
Eye Diagram	IEEE Std 802.3bm compatible					

Note:
1. The optical power is launched into OM3 MMF
2. Measured with a PRBS 2^{31}-1 test pattern @25.78125Gbps

Optical- Receiver

Parameter	Symbol	Min	Typ	Max	Unit	Note
Center Wavelength	λc	840	850	860	nm	-
Average Receiver Sensitivity (Pavg)	S	-	-	-10.3	dBm	1
Average Receiver Sensitivity (Pavg)	S	-	-	-7.5	dBm	2
Receiver Overload (Pavg)	POL	2.5	-	-	dBm	
Damage Threshold	POL	3.4	-	-	dBm	
Optical Reflectance	ORL	-	-	-12	dB	-
LOS De-Assert	LOSD	-	-	-11	dBm	-
LOS Assert	LOSA	-30	-	-	dBm	-
LOS Hysteresis	-	0.5	-	5	dB	-

Note:

1. Measured with PRBS 231-1 test pattern, 10.3125Gb/s and 25.78125Gb/s, BER<5E-5
2. Measured with PRBS 231-1 test pattern, 10.3125Gb/s and 25.78125Gb/s, BER<10-12

Electrical – Transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input Differential Impedance	ZIN	-	100	-	Ω	-
Differential Data Input Swing	VIN, P-P	180	-	900	mVP-P	-

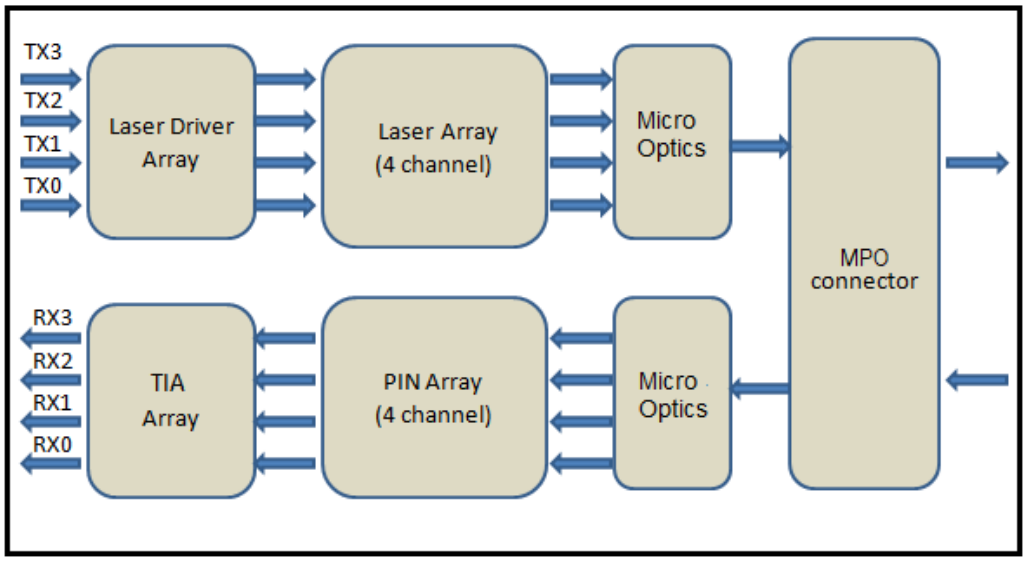
Electrical – Receiver

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output Differential Impedance	ZO	-	100	-	Ω	-
Differential Data Output Swing	VOUT, P-P	300	-	850	mVP-P	1
Transition Time (20% to 80%)	Tr,Tf	12			ps	

Notes:

1. Internally AC coupled, but requires external 100Ω differential load termination

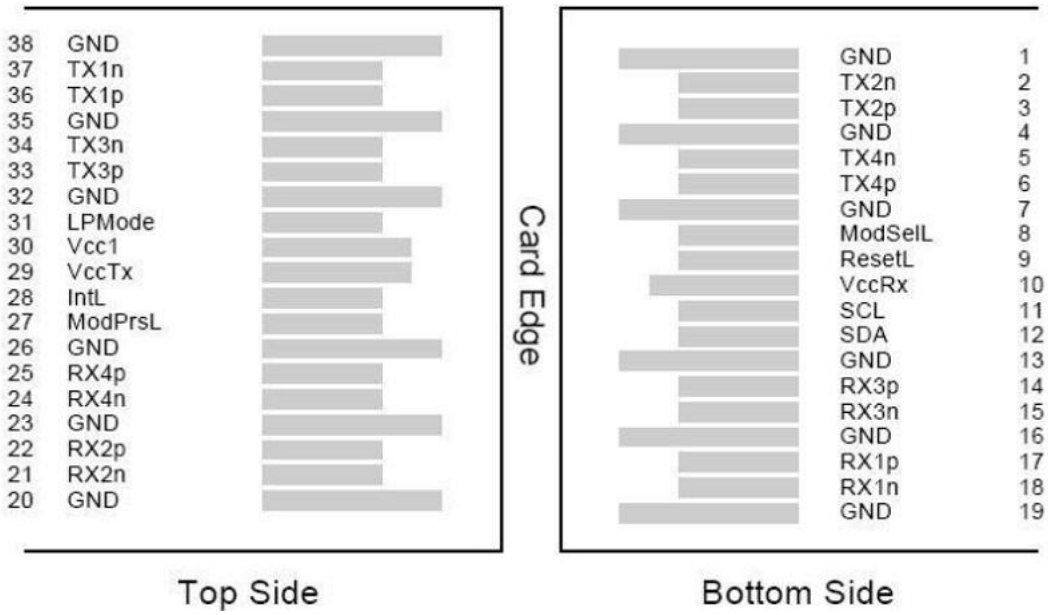
Transceiver Block Diagram



Functional Description

This product converts parallel electrical input signals into parallel optical signals, by a driven Vertical Cavity Surface Emitting Laser (VCSEL) array. The transmitter module accepts electrical input signals compatible with Common Mode Logic (CML) levels. All input data signals are differential and internally terminated. The receiver module converts parallel optical input signals via a photo detector array into parallel electrical output signals. The receiver module outputs electrical signals are also voltage compatible with Common Mode Logic (CML) levels. All data signals are differential and support a data rates up to 10.3125Gps@40G Mode/25.78Gbps@100G Mode per channel.

Electrical Connector Layout



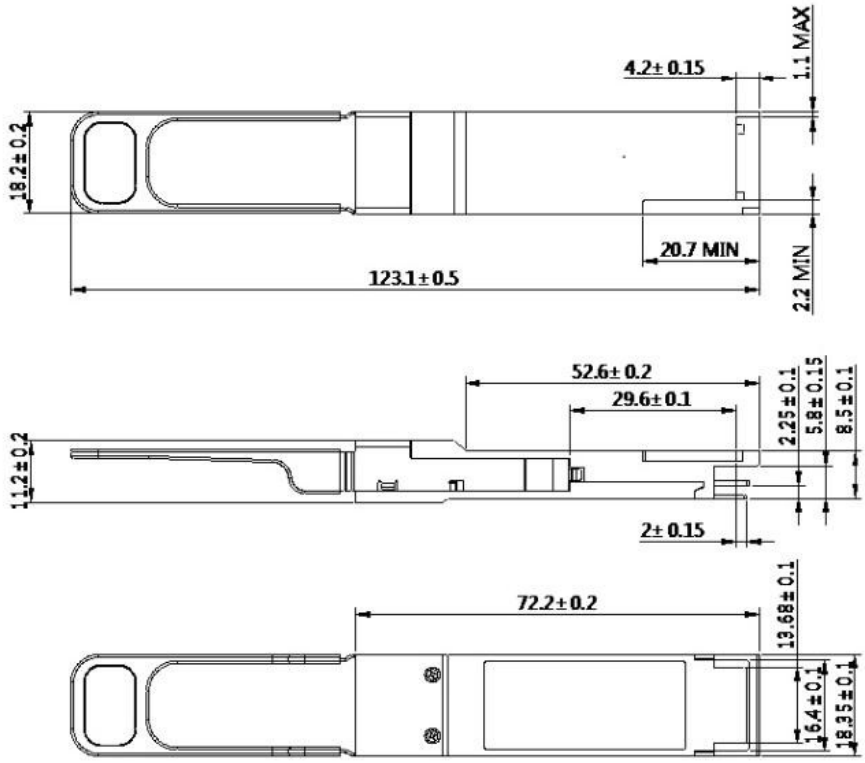
Electrical Pin Definition

PIN #	Symbol	Description	Remarks
1	GND	Ground	5
2	Tx2n	Transmitter Inverted Data Input, LAN2	
3	Tx2p	Transmitter Non-Inverted Data Input, LAN2	
4	GND	Ground	5
5	Tx4n	Transmitter Inverted Data Input, LAN4	
6	Tx4p	Transmitter Non-Inverted Data Input, LAN4	
7	GND	Ground	5
8	ModSelL	Module select pin, the module responds to two-wire serial communication when low level	1
9	ResetL	Module Reset	2
10	$V_{CC}RX$	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	5
14	Rx3p	Receiver Non-Inverted Data Output, LAN3	
15	Rx3n	Receiver Inverted Data Output, LAN3	
16	GND	Ground	5
17	Rx1p	Receiver Non-Inverted Data Output, LAN1	
18	Rx1n	Receiver Inverted Data Output, LAN1	
19	GND	Ground	5
20	GND	Ground	5
21	Rx2n	Receiver Inverted Data Output, LAN2	
22	Rx2p	Receiver Non-Inverted Data Output, LAN2	
23	GND	Ground	5
24	Rx4n	Receiver Inverted Data Output, LAN4	
25	Rx4p	Receiver Non-Inverted Data Output, LAN4	
26	GND	Ground	5
27	ModPrsL	The module is inserted into the indicate pin and grounded in the module.	3
28	IntL	Interrupt	4
29	$V_{CC}TX$	+3.3V Power Supply transmitter	
30	$V_{CC}1$	+3.3V Power Supply	
31	LPMode	Low Power Mode	5
32	GND	Ground	5
33	Tx3p	Transmitter Non-Inverted Data Input, LAN3	
34	Tx3n	Transmitter Inverted Data Input, LAN3	
35	GND	Ground	5
36	Tx1p	Transmitter Non-Inverted Data Input, LAN1	
37	Tx1n	Transmitter Inverted Data Input, LAN1	
38	GND	Ground	5

Notes:

1. ModSelL is the input pin. The module responds to 2-wire serial communication commands when it is held low by the host. ModSelL allows multiple QSFP modules to be used on a single 2-wire interface bus. If ModSelL is High, the module will not respond to any 2-wire interface communication from the host. ModSelL has internal pull-up resistors in the module
2. The module restart pin, when the low level on the ResetL pin lasts longer than the minimum pulse length, resets the module and restores all user modules to their default state. When performing reset device, the host should ignore all status bits. Until the module reset interrupt is completed, please note that during hot plugging, the module will issue this information to complete the reset interrupt without resetting
3. This pin is active high, indicating that the module is running under a low power module.
4. IntL is the output pin, which is the open collector output and must be pulled up to Vcc on the motherboard. When it is low, it indicates that the module may malfunction. The host uses a 2-wire serial interface to identify the interrupt source
5. Circuit ground is internally isolated from chassis ground.

Mechanical Dimensions



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