200G QSFP56 to 4 x 50G SFP56 DAC

Part Number: LBX-DB24S5Pyyy

LBX-DB24S5Pyyy 200G passive cable assembly provides high-speed, cost-effective alternatives to fiber optics in 4x50G Ethernet applications.

Features

- Compliant with QSFP56 MSA Specification Rev 3.4
- SFF-8679 electrical interface compliant
- SFF-8636 management interface support
- Support 50G (PAM4) electrical data rates/ channel
- 12C for EEPROM communication
- Pull to Release latch design
- Excellent EMI/ EMC performance
- 360-degree cable shield termination
- Advantage dual side pre-solder automated assembly technologies
- Low loss, stronger mechanical features, more flexible
- QSFP modules will be backwards compatible, allowing them to support existing QSFP modules and provide flexibility for end users and system designers

Applications

- Data Center & Networking Equipment
- Servers/ Storage Devices
- High Performance Computing (HPC)
- Switches/ Routers

Ordering Information

Part Number	Link Length
LBX-DB24S5P0P5	0.5m
LBX-DB24S5P001	1m
LBX-DB24S5P002	2m
LBX-DB24S5P003	3m

Product Overview

Vitex **LBX-DB24S5Pyyy** passive cable assembly offers next generation performance and is based on the industry standard specifications, such as SFF-8679, SFF-8636 and QSFP56 TO 4SFP56 MSA specification rev 4.0.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{STG}	-40	85	°C
Max Supply Voltage	$V_{CC}T$, R	-0.5	4	V

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	T_{OP}	0		70	°C
Power Supply Voltage	V_{CC}	3.14	3.3	3.47	V

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Power Dissipation	P			0.8	W

Electrical Pin Definition – QSFP56

Pin	Logic.	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	
12	LVCMOS-I/O	SDA	2-wire serial interface data	

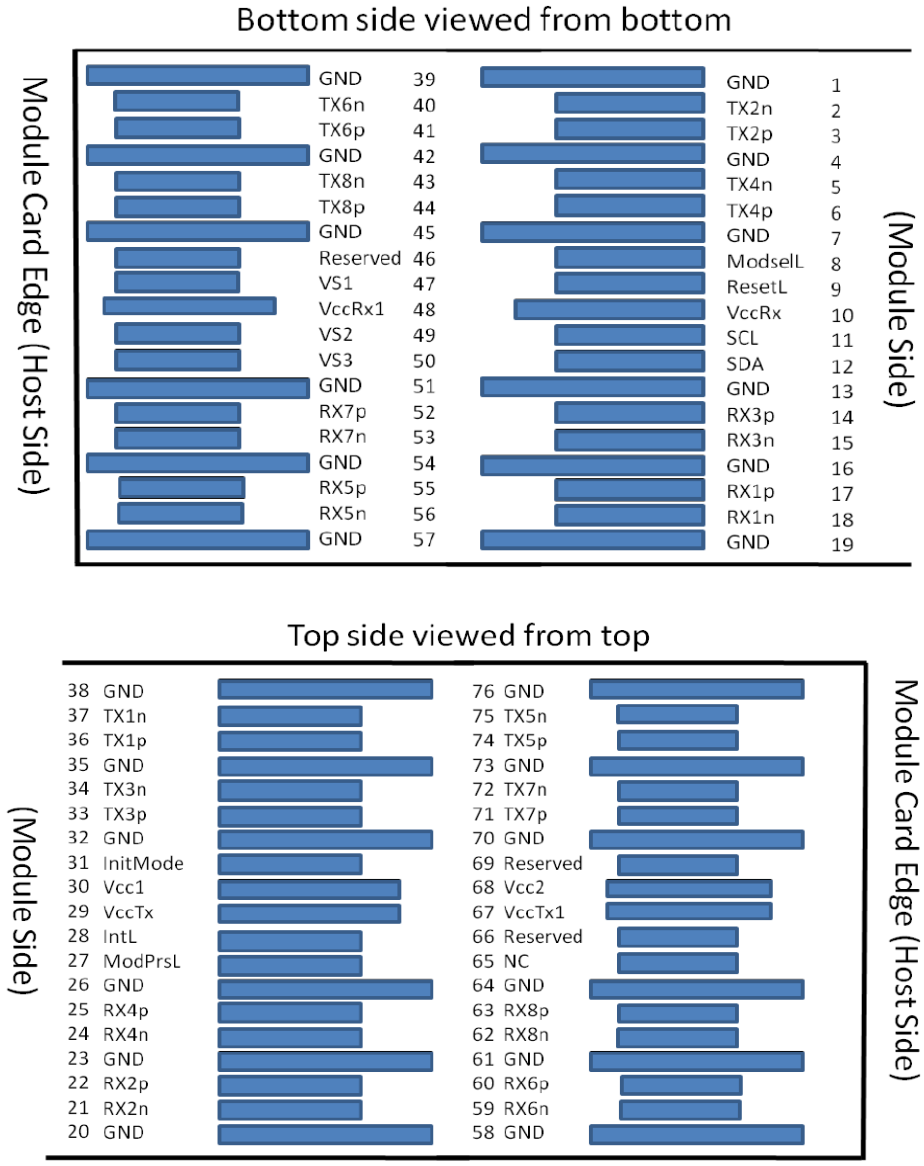
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vccl	+3.3V Power Supply	2
31	LVTTL-I	InitMode	Initialization mode: In legacy QSFP applications, the InitMode pad is called LPMODE	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	3
47		VSl	Module Vendor Specific 1	3
48		VccRx1	3.3V Power Supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	

53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69		Reserved	For future use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

Notes:

1. QSFP56 TO 2 QSFP uses common ground (GND)for all signals and supply (power). All are common within the QSFP56 TO 2 QSFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10K ohms and less than 100 pf.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP56 TO 2 QSFP pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

Electrical Connector Layout



Electrical Pin Definition -SFP56

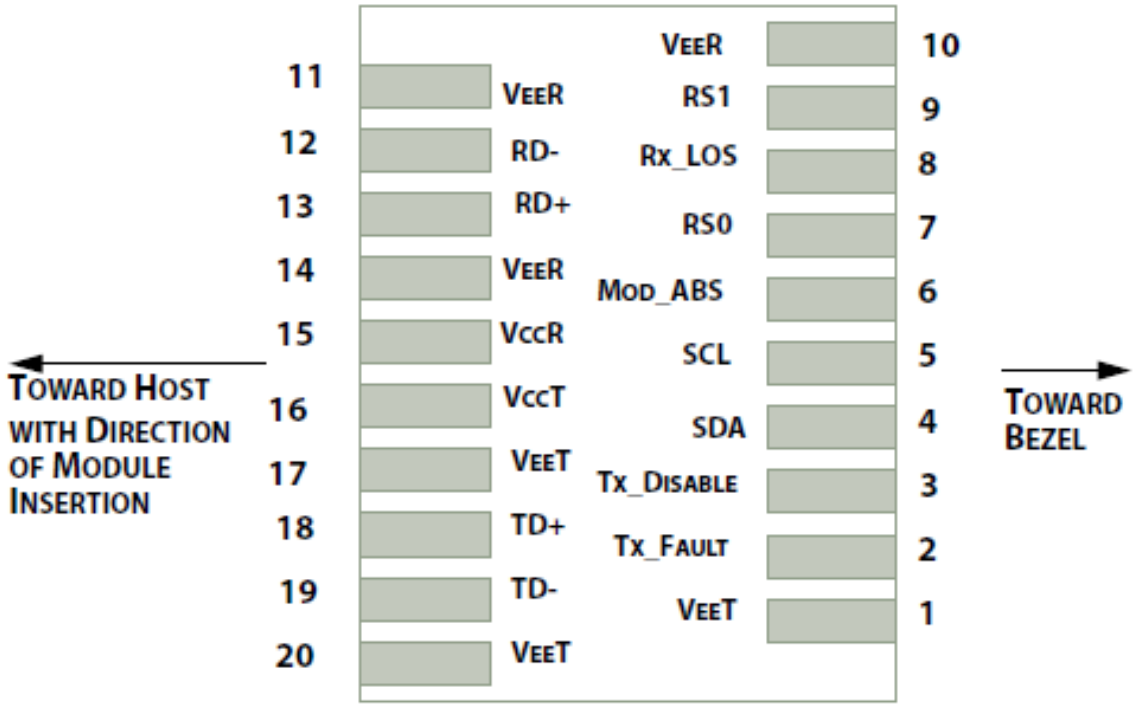
Pin	Logic.	Symbol	Name/Description	Note
1		VeeT	Transmitter Ground	
2	LV-TTL-O	TX_Fault	N/A	1
3	LV-TTL-I	TX_DIS	Transmitter Disable	2
4	LV-TTL-I/O	SDA	Tow Wire Serial Data	
5	LV-TTL-I	SCL	Tow Wire Serial	

6		MOD_DE	Module present,	
7	LV-TTL-I	RS0	N/A	1
8	LV-TTL-O	LOS	LOS of Signal	2
9	LV-TTL-I	RS1	N/A	1
10		VeeR	Receiver Ground	
11		VeeR	Receiver Ground	
12	CML-O	RD-	Receiver Data Inverted	
13	CML-O	RD+	Receiver Data	
14		VeeR	Receiver Ground	
15		VccR	Receiver Supply 3.3V	
16		VccT	Transmitter Supply	
17		VeeT	Transmitter Ground	
18	CML-I	TD+	Transmitter Data	
19	CML_I	TD-	Transmitter Data	
20		VeeT	Transmitter Ground	

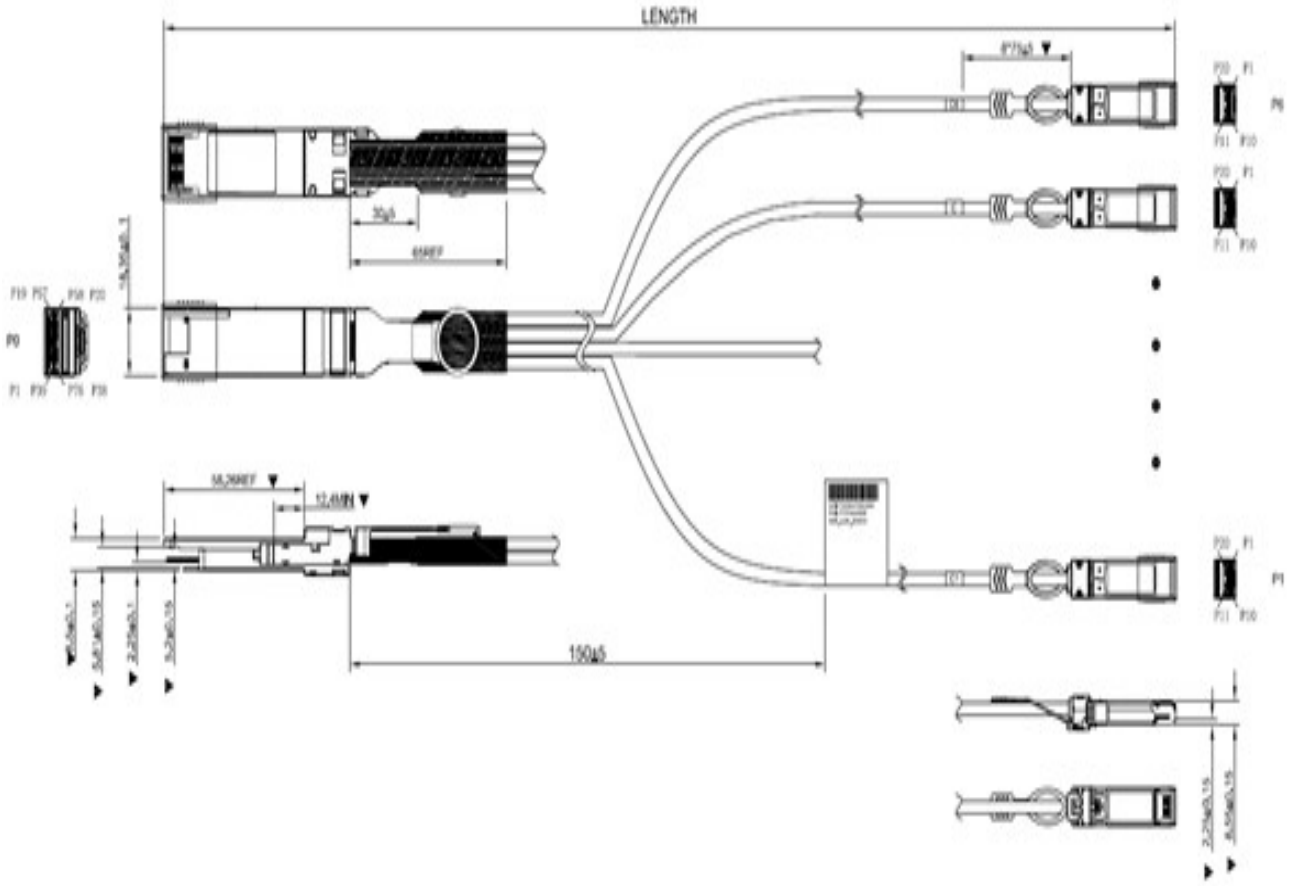
Notes:

1. Signals not supported in SFP56 Copper pulled down to VeeT with 30K ohms resistor.
2. Passive cable assemblies do not support LOS and TX_DIS

Electrical Connector Layout



Mechanical Dimensions



Contact Information

Vitex LLC
210 Sylvan Ave, Suite 25
Englewood Cliffs, NJ 07632
201-296-0145 | info@vitextech.com