200Gb/s QSFP56 SR4 70m OM3 Optical Transceiver

T-FX4FNS-N00

Product Specification

Features

- QSFP56 MSA compliant
- 4 parallel lanes on 850nm center wavelength
- Compliant to IEEE 802.3bs Specification
- Up to 100m transmission on multi-mode fiber (MMF) OM3 with FEC
- Operating case temperature: 0 to 70°C
- 4x53.125Gb/s electrical interface (200GAUI-4)
- Data Rate 53.125Gbps (PAM4) per channel.
- Maximum power consumption 5W
- MPO-12 APC connector
- RoHS compliant

Applications

- Data Center Interconnect
- 200G Ethernet
- Infiniband interconnects
- Enterprise networking

Part Number Ordering Information

T-FX4FNS-N00	200G QSFP56 SR4 70m OM3 with FEC optical transceiver with full real-time digital diagnostic monitoring and pull tab

1. General Description

This product is a parallel 200Gb/s Quad Small Form Factor Pluggable (QSFP56) optical module. It provides increased port density and total system cost savings. The design is compliant to IEEE802.3bs Annex120E (200GAUI-4 C2M). The QSFP56 full-duplex optical module offers 4 independent transmit and receive channels, each capable of 53.125Gb/s operation for an aggregate data rate of 200Gb/s on 70 meters of OM3 multi-mode fiber.

An optical fiber cable with an MTP/MPO-12 APC connector can be plugged into the QSFP56 SR4 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through a QSFP56 MSA-compliant edge type connector.

The central wavelengths of all the 4 parallel lanes are 850nm. It contains an optical MPO-12 APC connector for the optical interface and a 38-pin connector for the electrical interface. Host FEC is required to support up to 70m OM3 multi-mode fiber transmission.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP56 Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

2. Functional Description

The module incorporates 4 parallel channels, on 850nm Center Wavelength, operating at 50G per channel. The transmitter path incorporates a 4-channel CDR retimer, a quad channel VCSEL drivers together with a VCSEL array. On the receiver path, a photodiode array optics are coupled with an 4-channel CDR retimer. The electrical interface is compliant with IEEE 802.3bs and QSFP56 MSA in the transmitting and receiving directions, and the optical interface is compliant to QSFP56 MSA with MPO-12 APC Optical Connector. Figure 1 shows the functional block diagram of this product.

A single +3.3V power supply is required to power up this product. All the power supply pins are internally connected and should be applied concurrently. As per MSA specifications the module offers seven low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, InitMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product

indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Initialize Mode (InitMode) is an input signal. It is pulled up to Vcc in the QSFP56 module. The InitMode signal allows the host to define whether the QSFP56 module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in the QSFP56 Management Interface Specification. Under hardware control (InitMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. See SFF-8679 for LPMode signal description.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a "Low" state.

Interrupt (IntL) is an output pin. "Low" indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

3. Transceiver Block Diagram

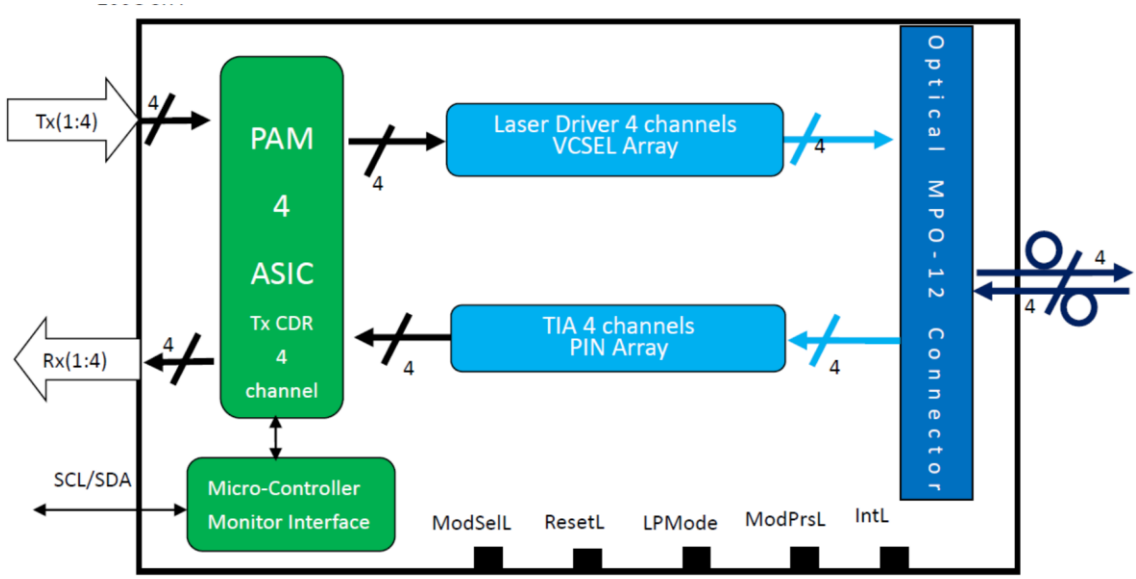

Figure 1. Transceiver Block Diagram

4. Optical interface and Pin Assignment

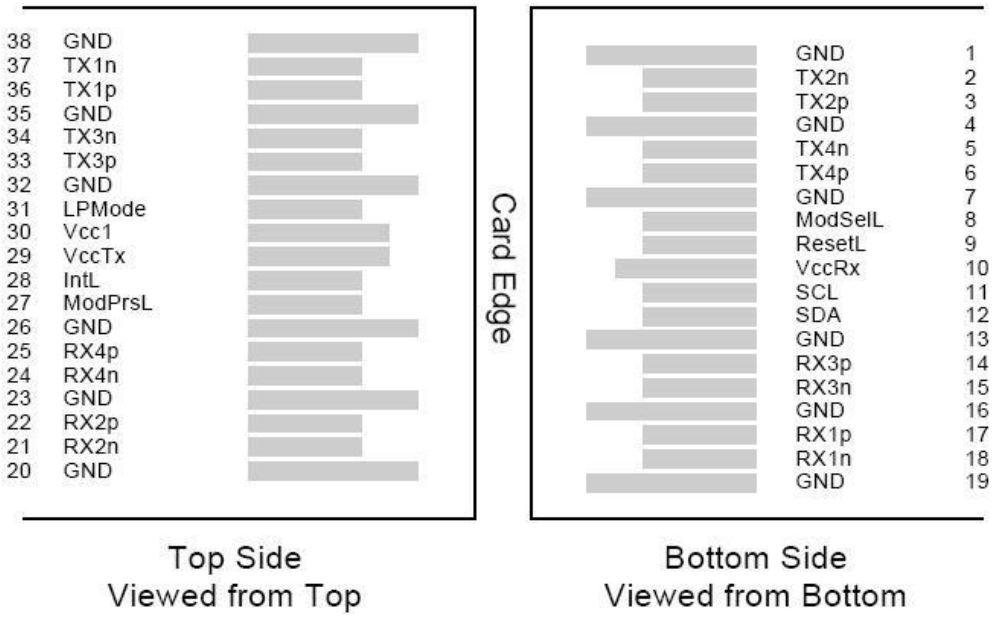

Figure 2. MSA Compliant Connector

5. Pin Definition

Pin Definition

PIN	Logic	Symbol	Name/Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	

37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Notes:

1. GND is the symbol for signal and supply (power) common for QSFP56 modules. All are common within the QSFP56 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 3 below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP56 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.

6. Recommended Power Supply Filter

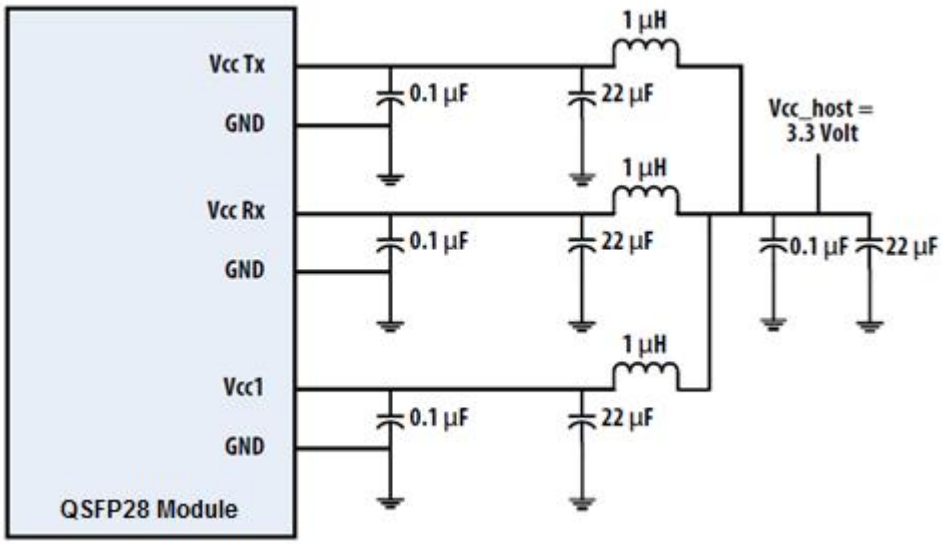

Figure 3. Recommended Power Supply Filter

7. Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-40	85	degC	
Operating Case Temperature	T_{OP}	0	70	degC	
Power Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	

8. Recommended Operating Conditions and Power Supply Requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	T_{OP}	0		70	degC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, each Lane			26.5625		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-12}$		1
Link Distance with OM3	D	0.5		100	m	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

9. Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Test Point	Min	Typical	Max	Units	Notes
Power Consumption				5	W	
Supply Current	Icc			1.52	A	
Transmitter (each Lane)						
Signaling Rate, each Lane	TP1	26.5625 ± 100 ppm			GBd	
Differential pk-pk Input Voltage Tolerance	TP1a	900			mVpp	1

Differential Termination Mismatch	TP1			10	%	
Differential Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1				2
Single-ended Voltage Tolerance Range (Min)	TP1a	-0.4 to 3.3			V	
DC Common Mode Input Voltage	TP1	-350		2850	mV	3
Receiver (each Lane)						
Signaling Rate, each lane	TP4	26.5625 ± 100 ppm			GBd	
Differential Peak-to-Peak Output Voltage	TP4			900	mVpp	
Common Mode vOLTAGE		-350		2850	mV	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-end Eye Height, Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	3

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

10. Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transmitter						
Center Wavelength	λ_C	840	850	860	nm	
Data Rate, each Lane		26.5625 ± 100 ppm			GBd	
Modulation Format		PAM4				
RMS Spectral Width	$\Delta\lambda_{rms}$			0.6	nm	Modulated
Average Launch Power, each Lane	P_{AVG}	-6.5		4	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	P_{OMA}	-4.5		3	dBm	2
Launch Power in OMA_{outer} minus TDECQ, each Lane		-5.9			dB	
Transmitter and Dispersion Eye Clouser for PAM4, each Lane	TDECQ			4.5	dB	
Extinction Ratio	ER	3			dB	
Optical Return Loss Tolerance	TOL			12	dB	
Average Launch Power of OFF Transmitter, each Lane	P_{off}			-30	dBm	
Encircled Flux		≥ 86% at 19 μm ≤ 30% at 4.5 μm				
Receiver						
Center Wavelength	λ_C	840	850	860	nm	
Data Rate, each Lane		26.5625 ± 100 ppm			GBd	
Modulation Format		PAM4				
Damage Threshold, each Lane	TH_d	5			dBm	3

Average Receive Power, each Lane		-8.4		4	dBm	4
Receive Power (OMA_{outer}), each Lane				3	dBm	
Receiver Sensitivity (OMA_{outer}), each Lane	SEN			Equation1	dBm	7
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS			-3.4	dBm	5
Receiver Reflectance	R_R			-12	dB	
LOS Assert	LOSA	-30			dBm	
LOS De-assert	LOSD			-12	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Stressed Conditions for Stress Receiver Sensitivity (Note 7)						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			4.5		dB	
SECQ – 10log10(*C*eq)f (max), lane under test			4.5		dB	
OMA_{outer} of each Aggressor Lane			3		dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ < 1 dB , the OMA_{outer} (min) must exceed the minimum value specified here.
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Measured with conformance test signal at receiver input for the BER of $2.4x10^{-4}$.
6. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
7. Receiver sensitivity

Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.5 dB. Receiver sensitivity should meet Equation (1), which is illustrated in Figure 1.

$$RS = \max(-6.5, SECQ - 7.9) \text{ (dBm)} \quad \text{(Equation 1)}$$

where

RS is the receiver sensitivity

SECQ is the SECQ of the transmitter used to measure the receiver sensitivity

The normative requirement for receivers is stressed receiver sensitivity.

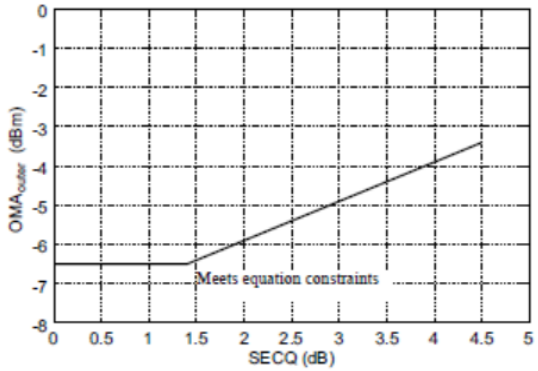

Figure 4. Illustration of receiver sensitivity

11. Digital Diagnostic Functions

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

12. Mechanical Dimensions

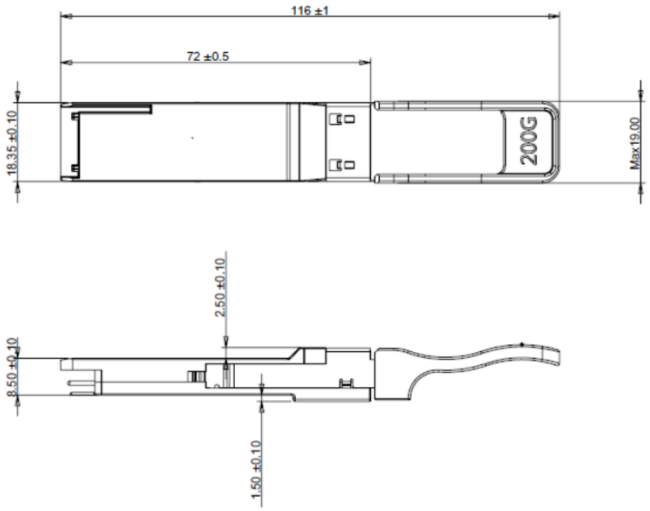

Figure 5. Mechanical Outline

13. ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment

14. Laser Safety

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

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