200G QSFP DD PSM8 Optical Transceiver

Part Number: VQ-2CLR8CP-AA

VQ-2CLR8CP-AA is a high performance QSFP DD transceiver module for 200 Gigabit Ethernet data links over single mode fiber.

Features

- 8 channels full-duplex transceiver modules
- Supports 8×25Gb/s aggregate bit rates
- Supports 8×10Gb/s aggregate bit rates if required
- 8 channels 1310nm DFB
- 8 channels PIN photo detector array
- Internal CDR circuits on both receiver and transmitter channels
- Support CDR bypass
- Low power consumption <6W
- Hot Pluggable QSFP DD form factor
- Up to 2km reach for G.652 SMF
- Single male MPO (APC 8-degree) connector receptacle
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- RoHS 2.0 compliant (lead free)

Applications

- 2×100G Ethernet links
- Infiniband DDR/EDR
- Datacenter and Enterprise networking

Ordering Information

Part Number	Data Rate	Link Length	Laser	Detector	Fiber Type	Temperature
VQ-2CLR8CP-AA	200G	2 km for G.652 SMF	1310nm DFB	1310nm PIN array	SMF	0 – 70°C

Product Overview

Vitex **VQ-2CLR8CP-AA** is an Eight-Channel, Pluggable, Parallel, Fiber-Optic QSFP DD PSM8 for 2×100 Gigabit Ethernet, Infiniband DDR/EDR Applications. This transceiver is a high-performance module for data communication and interconnect applications. It integrates eight data lanes in each direction with 208 Gbps bandwidth. Each lane can operate at 26Gbps up to 2km over G.652 SMF. These modules are designed to operate over single mode fiber systems using a nominal wavelength of 1310nm. The electrical interface uses a 76-contact edge type connector. The optical interface uses a 24 fiber MTP (MPO) connector.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{cc}	-0.3	3.6	V
Input Voltage	V_{in}	-0.3	V_{cc} + 0.3	V
Storage Temperature	T_s	-20	85	°C
Case Operating Temperature	T_c	0	70	°C
Humidity (non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{cc}	3.13	3.3	3.47	V
Operating Case Temperature	T_c	0		70	°C
Baud Rate per Lane	f_d	10.3125	25.78125		Gbps
Humidity	Rh	5		85	%
Power Dissipation	P_m		5.28	6	W
Fiber Bend Radius	R_b	0.002		2	km

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Z_{in}	90	100	110	ohm
Differential Output Impedance	Z_{out}	90	100	110	ohm
Differential Input Voltage Amplitude [1]	ΔV_{in}	190		700	mV_{pp}
Differential Output Voltage Amplitude [2]	ΔV_{out}	300		850	mV_{pp}
Input Logic Level High	V_{IH}	2.0		V_{cc}	V
Input Logic Level Low	V_{IL}	0		0.8	V
Output Logic Level High	V_{OH}	V_{cc} – 0.5		V_{cc}	V
Output Logic Level Low	V_{OL}	0		0.4	V

Note:
1: Differential input voltage amplitude is measured between TxnP and TxnN.
2: Differential output voltage amplitude is measured between RxnP and RxnN.

Optical – Transmitter

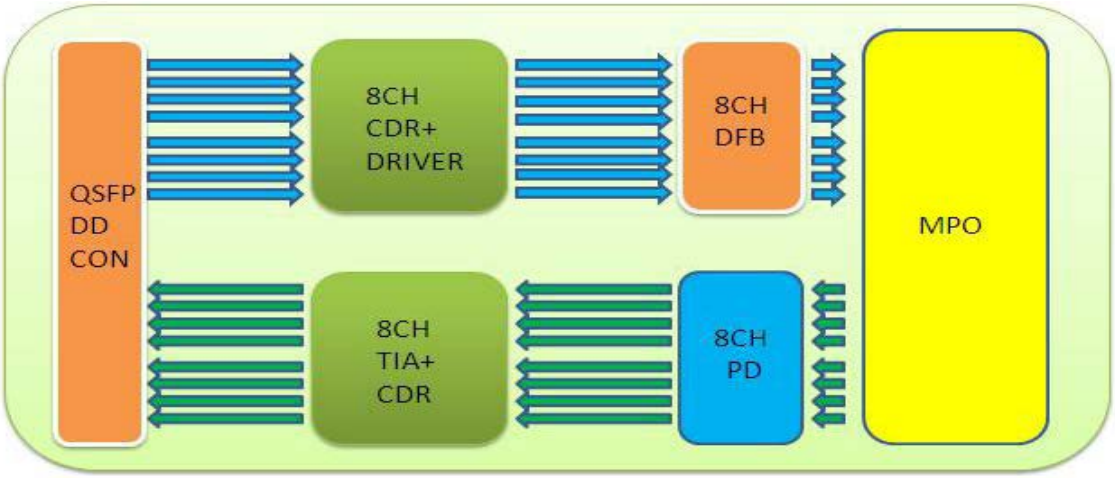
Parameter	Symbol	Min	Typical	Max	Unit
Center Wavelength	λ_c	1295	1310	1325	nm
Side Mode Suppression Ratio	SMSR	30	-		dB
Average Launch Power (each lane)	PAVG	-6	-	2	dBm
Optical Modulation Amplitude (each lane)	POMA	-5.0		2.2	dBm
TDP, each lane	TDP			2.9	dB
Extinction Ratio	ER	3.5			dB
Relative Intensity Noise	RIN			-128	dB/Hz
Optical Return Loss Tolerance	TOL			20	dB
Transmitter Reflectance	RT			-12	dB
Average Launch Power of OFF Transmitter (each lane)	POFF			-30	dB
Eye Mask Coordinates1: X1, X2, X3, Y1, Y2, Y3	{0.31,0.4,0.45,0.34,0.38,0.4} Hit Ratio = 5x10-5				

Optical – Receiver

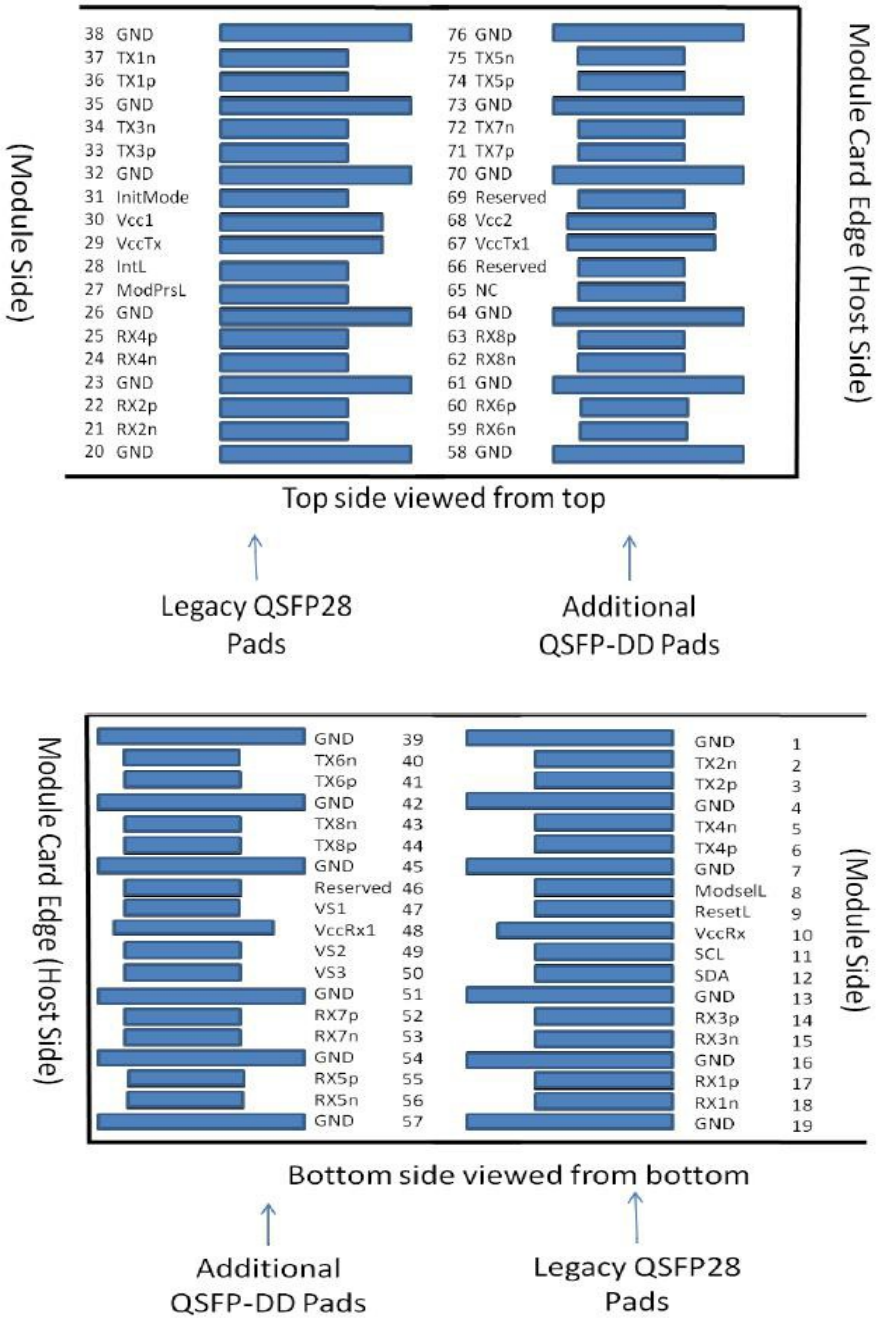
Parameter	Symbol	Min	Typical	Max	Unit
Center Wavelength	λ_c	1295	1310	1325	nm
Damage Threshold, each lane	THd	3.0			dBm
Average Receive Power,each lane		-12.66		2.0	dBm
Receive power, each lane (OMA) (max)				2.2	dBm
Receiver Reflectance	RR			-26	dBm
Receiver Sensitivity (OMA), each lane	SEN			-11.35	dBm
LOS Assert	LOSA		-18		dBm
LOS De-Assert – OMA	LOSD		-15		dBm
LOS Hysteresis	LOSH	0.5		3	dB

Note:
1: Even if the TDP<1dB,the OMA min must exceed the minimum value specified here.
2: The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
3: Sensitivity is specified at 5x10^-5 BER at 25.78125Gb/s.

Block Diagram



Electrical Connector Layout



Electrical Pin Definition

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

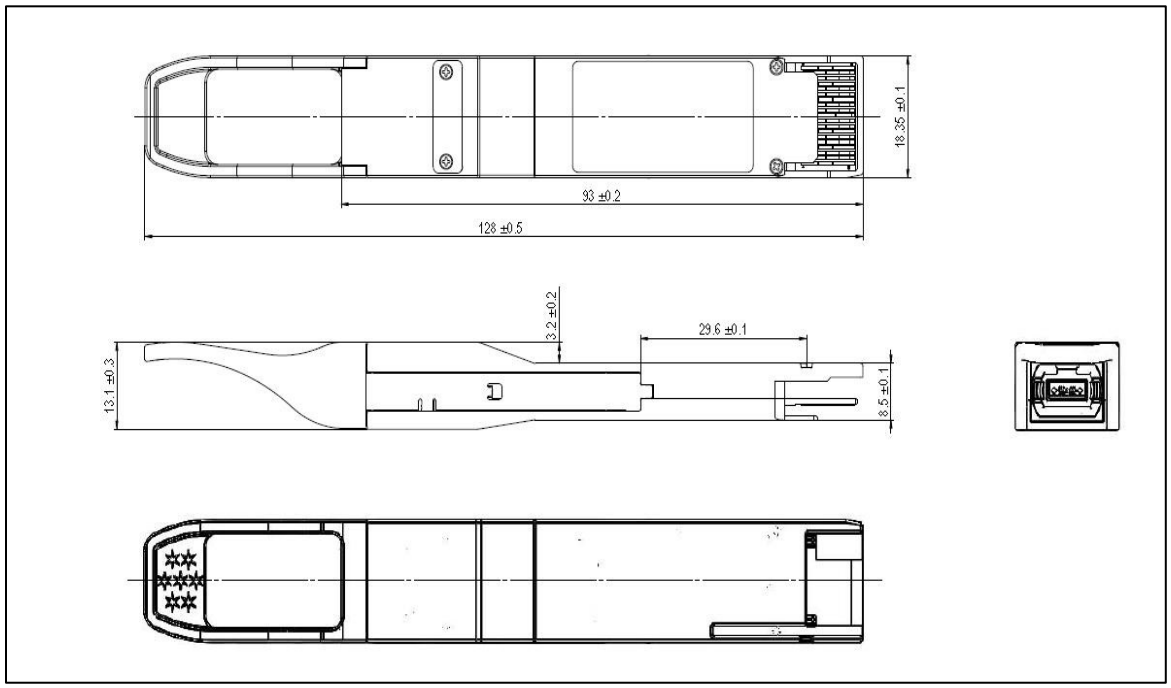
Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

References

1. QSFP DD MAS Rev4.0
2. Ethernet 100GBASE-PSM4 IEEE802.3bm

Mechanical Dimensions



Contact Information

Vitex LLC
210 Sylvan Ave, Suite 25
Englewood Cliffs, NJ 07632
201-296-0145 | info@vitextech.com
www.vitextech.com